Serial No.: 10/605,100	Art Unit: 2818
------------------------	----------------

## **IN THE ABSTRACT**

Please amend the abstract to read as follows:

-- In an SOI MOSFET device with a silicon layer formed on a dielectric layer, a gate electrode stack is formed with sidewall spacers composed of sidewall spacer material on sidewalls of the gate electrode stack. Raised source/drain regions are formed on the surface of the silicon layer. The gate electrode stack comprises a gate electrode formed of polysilicon over a gate dielectric layer formed on the surface of the silicon layer. A plug of dielectric material which may comprise sidewall spacer material fills a notch on the edges of a cap layer above the gate polysilicon and beneath a hard mask layer that overlies the cap layer. The sidewalls of the gate electrode are covered by the sidewall spacers which cover a portion of the plug for the purpose of eliminating the exposure of the gate polysilicon, so that to avoid formation of spurious epitaxial growth during the formation of raised source/drain regions. is avoided. --